Contact resistivity measurements of the buried Si-ZnO:Al interface of polycrystalline silicon thin-film solar cells on ZnO:Al

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Abstract

An experimental method is developed for contact resistivity measurements of a buried interface in polycrystalline silicon (poly-Si) thin-film solar cell devices on aluminum doped zinc oxide (ZnO:Al) layers. The solar cell concept comprises a glass substrate covered with a temperature-stable ZnO:Al film as transparent front contact layer, a poly-Si n+/p-/p+ cell, as well as a metal back contact. Glass/ZnO:Al/poly-Si/metal test stripe structures are fabricated by photolithographic techniques with the ZnO:Al stripes locally bared by laser ablation. The high-temperature treatments during poly-Si fabrication, e.g. a several hours lasting high-temperature step at 600°C, are found to have no detrimental impact on the ZnO:Al/Si interface contact resistivity. All measured ρ_C values range well below 0.4 Ωcm^2 corresponding to a relative power loss ΔP below 3% for a solar cell with 500mV open circuit voltage and 30mA/cm^2 short circuit current density. By inclusion of a silicon nitride (SiN_x) diffusion barrier between ZnO:Al and poly-Si the electrical material quality of the poly-Si absorber can be significantly enhanced. Even in this case, the contact resistivity remains below 0.4 Ωcm^2 if the diffusion barrier has a thickness smaller than 10nm.

1 Introduction

Thin-film solar cells based on polycrystalline silicon (poly-Si) combine the low-cost aspects of thin-film technology with the high electrical material quality of crystalline silicon. Solar grade poly-Si absorber layers can be fabricated by thermal solid phase crystallization (SPC) of amorphous silicon on foreign substrates [1,2]. Poly-Si thin-film solar cells on glass substrate with more than 10% efficiency could be demonstrated by CSG solar [3]. In this case, the silicon was deposited by plasma enhanced chemical vapour deposition (PECVD) and subsequently solid phase crystallized by a several hours lasting thermal annealing step at 600°C. Two other high-temperature processes, a rapid thermal annealing process at about 950°C for some seconds and hydrogen passivation at about 600°C, follow. However, sophistically etched structures are used in these devices from CSG solar for contacting and series connection of the solar cells. An alternative poly-Si thin-film solar cell approach uses aluminum doped zinc oxide (ZnO:Al) films on glass as transparent front contact layers [4] which are already widely used in a-Si:H/µc-Si:H technology [5,6]. The structure of the poly-Si/ZnO:Al solar cell device is shown in Fig. 1. The use of a ZnO:Al film as transparent conductive front contact in the poly-Si thin-film solar cell device not only allows for an easy contacting scheme via laser scribing, but also affords light trapping by texturing ZnO:Al layer surface. The ZnO:Al films were found to be stable upon high temperature-treatments during poly-Si preparation [7]. If capped with silicon, the carrier mobilities of the ZnO:Al layers can be strongly improved from 42 cm^2/Vs to 67 cm^2/Vs with nearly constant carrier density after heat-treatment, leading to a strong decrease of the ZnO:Al sheet resistance [8].

However, while the electrical and optical properties of the underlying ZnO:Al layer itself are fairly known, little has been investigated about the electrical performance of the buried poly-Si/ZnO:Al interface. The main questions are: What is the impact of high-temperature treatments on the contact resistance of the interface? Will there form an isolating barrier? What is the optimum surface treatment of the ZnO:Al layer before silicon deposition? To which extent will a diffusion barrier between ZnO and silicon affect the contact resistance? Such a barrier might be necessary to avoid the diffusion of impurities from the glass substrate and the ZnO:Al film into the silicon during high-temperature steps. In poly-Si thin-film solar cell technology most commonly silicon nitride (SiN_x) is used as barrier [9]; for a-Si:H solar cells also thin Ge layers are employed [10].

In this study, we characterize the buried ZnO:Al-Si interface by measuring the contact resistivity by a method similar to an earlier work by Schade and Smith [11] and by the well-known transmission line method [12,13]. Hereby, metal/poly-Si/(SiN_x)/ZnO:Al/glass stacks are fabricated with the ZnO:Al and metal contacts structured into single stripes by photolithographic techniques.

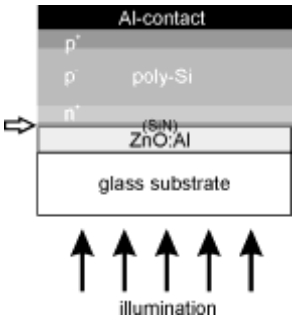

Figure 1: Structure of the polycrystalline silicon thin-film solar cell on ZnO:Al-coated glass. The buried interface under investigation is marked by a white block arrow.

2 Theory

The electrical performance of a contact interface in the thin-film solar cell device can be characterized by the specific contact resistivity

(1) $$\rho_c = R_C \cdot A$$

with R_C and A being the contact resistance (in Ohm) and the contact area (in cm^2). This formula implies a homogeneous current density over the whole contact area which is the case for a vertical current flow (Fig. 2, a)).

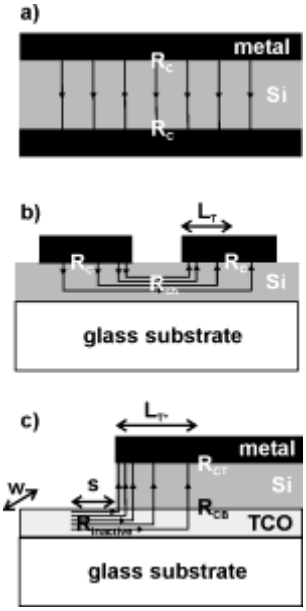

Figure 2: Three different configurations for the measurement of contact resistances in silicon thin-film devices. a) Homogeneous current flow through a silicon film sandwiched by two metal contacts with contact resistance R_C (difficult to realize experimentally), b) inhomogeneous current flow through a TLM structure for the determination of the silicon-metal contact resistance R_C with R_{sh} denoting the silicon sheet resistance and L_T the corresponding transfer length, c) structure proposed by Schade and Smith for the determination of a buried bottom contact resistance R_{CB} with R_{CT} indicating the metal-silicon top contact resistance and $R_{inactive}$ the resistance in the TCO layer for the distance s of the contact needle from the metal stripe. The width of the contact stripes is given by w, the transfer length by L_{T*}.

However, in thin-film technology there is often a situation where electrical transport happens *horizontally* through a layer with finite sheet resistance R_{sh} with metal contact pads placed on top of this layer. In this case, the current density through the interface isn't homogeneous anymore and decays exponentially from the edge of the contact pad. A transfer length L_T can be defined describing the distance from the contact edge where the current density has decreased to 1/e of its initial value directly at the front edge, provided that the width of the contact is much larger than L_T. (Fig. 2, b)). The contact resistivity can be extracted by the well-known transmission line model (TLM) using contact stripes placed on the film with variable distances from each other [10,11]. The contact resistivity ρ_C is defined in this case by

(2) $$\rho_c = R_{sh} \cdot L_T^2$$

For the determination of the contact resistivity of a buried ZnO:Al/Si interface a ZnO:Al/Si/metal layer stack is necessary. If the ZnO:Al has a finite sheet resistance $R_{sh/ZnO}$, there is an inhomogeneous current flow through both interfaces (Fig. 2, c)). Again a transfer length L_{T*} can be defined. Assuming a negligible resistance of the Si-layer, the sum of both interface resistivities can be defined by

(3) $$\rho_{cT} + \rho_{cB} = R_{sh/ZnO} \cdot L_{T*}^2$$

with ρ_{cT} denoting the resistivity of the top metal-silicon interface and ρ_{cB} the resistivity of the bottom silicon-ZnO:Al interface. The transfer length L_{T*} can be experimentally yielded by

(4) $$\frac{R(l)}{R(l/2)} = \frac{1}{2}\left[1 + \tanh^2\left(\frac{l}{2L_{T*}}\right)\right]$$

with $R(l)$ and $R(l/2)$ being the resistances measured through the whole stack with metal stripes of the lengths l and l/2 [11]. The measured IV-characteristics will also include an additional resistance $R_{inactive}$ due to the fact that the contact finger cannot be placed directly below the metal stripe but has to be positioned on the bared part of the ZnO:Al stripe. Therefore the total resistance is given by $R_{total} = U/I = R_{inactive} + R_{CB} + R_{CT}$. Before applying equation (4), $R_{inactive}$ has to be calculated by $R_{sh/ZnO} \cdot s/w$ with s being the distance of the contact finger from the metal pad and w the width of contact stripes, and has to be subtracted from R_{total} in advance. In case of L_{T*} being larger than the length of the metal stripe, an upper limit of $\rho_{CB} + \rho_{CT}$ can be calculated by assuming a homogeneous current flow through the whole contact area by applying equation (1).

3 Experimental

3.1 Sample preparation

Corning Eagle glass covered by an about 800nm thick ZnO:Al layer was used as substrate for the contact resistivity test structures as well as for solar cell devices. The ZnO:Al was prepared at a substrate temperature of 300°C by non-reactive radio frequency (RF) magnetron sputtering using a ceramic target with 1 wt% Al_2O_3 content [12]. Some ZnO:Al layers were subsequently covered by a 10-50nm thick SiN layer prepared by PECVD.
The first preparation step of contact resistivity test structures was the fabrication of equally spaced ZnO:Al stripes on glass (left side of Fig. 3). For that, the ZnO:Al film was covered by photolithographically structured photoresist. In a second step, the residual of the film was etched away by 1% hydrochloric acid (HCl) in case a bare ZnO:Al and 1% hydrofluoric acid (HF) in case of SiN-covered ZnO:Al. The photoresist was removed by aceton afterwards. Some of the bare ZnO:Al stripe surfaces were further textured by a 13 second 0.5% HCl etching step similar to light trapping structures for a-Si:H thin-film solar cells [6]. The sheet resistances of the ZnO:Al layers are 4 Ω˝ for smooth and 5.2 Ω˝ for textured films respectively at this stage of preparation.

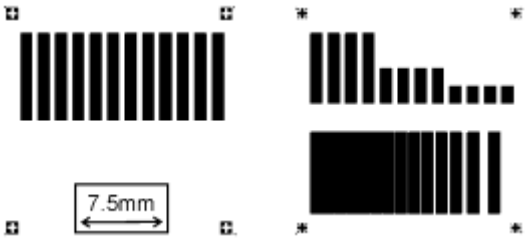

Figure 3: Photolithography masks for structuring the underlying ZnO:Al stripes with 1x7.5mm^2 size (left side) and the aluminium contacts on top with 1mm width and 6, 3 and 1.5mm length (right side). A TLM structure is included for extraction of the top contact resistivity (right bottom) with bar distances ranging between 10 and 800µm and a bar length 7.5mm.

Subsequently the whole sample surface was covered by amorphous silicon films of about 300-500nm thickness. N-type silicon layers were deposited by PECVD and p-type layers were prepared by both, PECVD and electron-beam evaporation. Some of the structures were subsequently solid phase crystallized by a 15 hours lasting annealing step at 600°C in a tube furnace at N_2 atmosphere. This SPC step equals the solar cell fabrication process in order to be sure that the ZnO:Al/Si interface of the test structures undergoes the same process conditions like solar cells. By this annealing step, the resistivity of the underlying ZnO:Al decreases by more than 40% such that the sheet resistances decline to about 2.1 Ω˝ for smooth and 2.8 Ω˝ for textured films respectively.
By a second photolithography and lift-off process, aluminium (Al) structures were deposited on top. Al stripes of different lengths were well aligned above the ZnO:Al structures. Additionally a TLM structure with bar distances ranging from 10 to 800µm was fabricated aside, in order to have the ability to determine the Al/Si contact separately. The length of the bars is 7.5mm. Before metallization, the native oxide on the silicon layer was removed by a 1% HF-dip.
In order to be able to electrically contact the underlying ZnO:Al stripes, the silicon was locally removed. For this purpose, a frequency doubled, optically pumped solid-state laser (Nd:YAG) at a wavelength of 532 nm was used for laser ablation. The pulse length and energy was about 10ns and 63µJ respectively. The final structure is shown in Fig. 4.

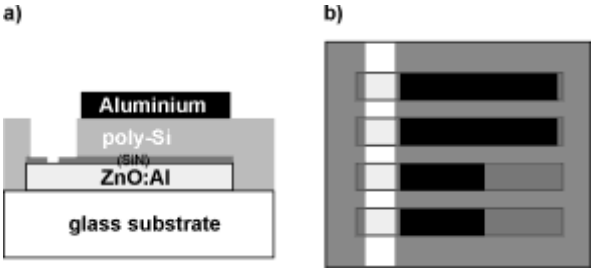

Figure 4: Contact stripe structure for the measurement of a buried ZnO:Al/poly-Si interface a) side view, b) top view.

Solar cells in n+/p-/p+ configuration were prepared on ZnO:Al by SPC of amorphous silicon. Details of the fabrication process can be found elsewhere [4].

3.2 Characterization methods

IV-measurements

Current-voltage characteristics were measured by automatic control and readout of a "238 High-Current Source-Measure Unit" from Keithley. The test structures were contacted by four gold needles with spherical tip in order to avoid penetration through the thin films and thus causing a shunt. To be sure that the samples don't burn through, the measurements are performed in the current-driven mode, i.e. the current is imposed by two needles while the voltage is picked off by the other two needles. The four-point setup also allows for more sophisticated measurement configurations with the current imposed through the whole layer stack while the voltage is picked off at different places (Fig. 5). In this way, the contributions from the ZnO:Al/Si and Si/Al interface to the overall contact resistivity can be separated from each other. As U_{probe} measured at an adjacent metal stripe denotes the spatial mean of the potential in the silicon layer [11], the top contact resistance R_{CT} can be determined separately by $(U_{TB}-U_{probe})/I_{TB}$ and the sum $R_{inactive} + R_{CB}$ can be calculated by U_{probe}/I_{TB} with I_{TB} being the current imposed through the whole layer stack and U_{TB} being the corresponding measured voltage.

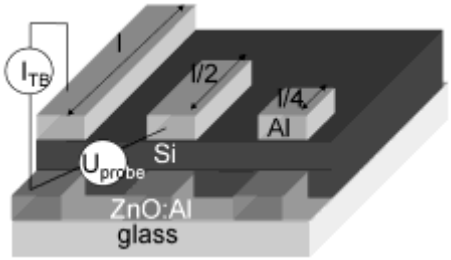

Figure 5: Schematic drawing of the four point measurement configuration. The inhomogeneous current flow through the contact area due to $R_{sh,\,Zno}$ is addressed by different contact pad lengths. The measurement of U_{probe} allows for an alternative determination of R_{CT} and $R_{inactive} + R_{CB}$.

Hall- and four-point-probe measurements

Hall-measurements in van der Pauw geometry yield information about the free carrier density in the silicon layers as well as the sheet resistance of silicon-capped ZnO:Al layers after annealing, e.g. for the calculation of $R_{inactive}$,. Alternatively, the sheet resistance of the ZnO:Al layers is also determined by four-point-probe measurements.

4 Results

4.1 Contact resistivity of the Si/Al interface

The Si/Al interface resistivity was determined by default by the TLM structure placed on each sample (Fig. 3 right bottom). A typical TLM characteristic for an Al-contact on n^+-doped poly-Si (1.7E20cm^{-3}) with 320nm thickness is shown in Fig. 6. A contact resistivity ρ_C = (2.8 ± 1.5) µΩcm^2 and a poly-Si sheet resistance R_{sh} = (23.3 ± 0.4) Ω$_{\square}$ could be extracted with corresponding transfer length L_T = 3.5 µm. It can be seen that the minimum fabricable metal bar distance of 10µm is hardly sufficient for an accurate extraction of ρ_C in this case. Bar distances in the order of the transfer length would favour a more accurate measurement. However, in most cases an upper limit for ρ_C could be determined.

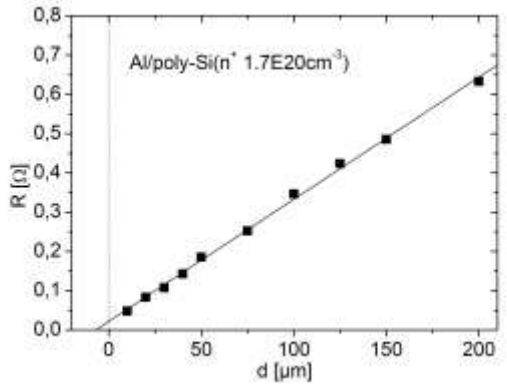

Figure 6: TLM measurement of an Al/poly-Si(n+) contact. The thickness of the poly-Si(n+) layer is 320nm.

The Si/Al resistivity could also be measured by U_{probe} in four-point configuration on the ZnO:Al/Si/Al test stripe structures as described in section 3.2. If an accurate determination of ρ_C by TLM was not possible because of geometrical limitations of the structure, the U_{probe} method was consulted.
The highest values measured for all Al/Si interfaces are summarized in Table 1. Please note that these maximum values are not limited by the physics of the interface but rather by the resolution of the respective measurement. Nevertheless, knowledge about the Al/Si contact resistivity is necessary for the determination of ρ_C of the buried Si/ZnO:Al interface described in the next section.

Interface	ρ_C [mΩcm^2]	Method
Al/poly-Si(n^+, ~1E20cm^{-3})	0.003 - 0.1	TLM
Al/poly-Si(p^+, ~1E19cm^{-3})	< 5	TLM
Al/a-Si(p^+, ~1E17cm^{-3})	< 20	U_{probe}
Al/a-Si(n^+, ~1E18cm^{-3})	Non-ohmic	TLM

Table 1: Upper limits for the contact resistivity of Al/Si interfaces for different types of silicon. The measurement method is given in the third column.

4.2. Contact resistivity of the buried ZnO:Al/Si interface

Influence of the high-temperature crystallization process

Figure 7 shows the IV-characteristics measured through a ZnO:Al/a-Si(p^+, ~1E17cm^{-3})/Al stack for 1.5mm, 3mm and 6mm long contact stripes. The silicon layer has been deposited by electron-beam evaporation at a temperature of 300°C and has a thickness about 340nm. The linear characteristic indicates an ohmic resistance. As the contact finger on the ZnO:Al-pad was displaced by 0.34mm from the metal contact $R_{inactive} = R_{sh/ZnO} \cdot s/w$ = 4 Ω · 0.34mm/1mm = 1.34 Ω which is much smaller than $R_{total} = R_{inactive} + R_{CB} + R_{CT}$ with values larger than 20Ω. The transfer length L_{T*} can be calculated by equation (4) to (2.70 ± 0.10) mm resulting in a total contact resistivity $\rho_{CT} + \rho_{CB}$ = (292 ± 22) mΩcm^2. In order to certify this value, we also made an overestimation by assuming a homogeneous current flow through the whole contact area of the shortest metal pad (l = 1.5mm) by measuring U_{probe} and I_{TB} resulting in about 340 mΩcm^2. As the top contact resistivity ρ_{CT}, measured by TLM, ismore than one order of magnitude smaller (see Table 1), these values can be taken as an upper limit for ρ_{CB} of the buried ZnO:Al/a-Si(p^+) interface.

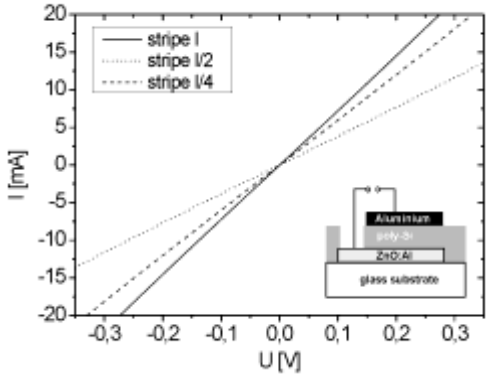

Figure 7: IV-characteristics measured through ZnO:Al/ a-Si(p^+)/Al stacks with three different Al contact stripe lengths resulting in a transfer length L_T = (2.70 ± 0.10)mm and a total contact resistivity $\rho_{CT} + \rho_{CB}$= (292 ± 22)mΩcm^2.

The corresponding IV-characteristics of a ZnO:Al/poly-Si(p^+~1E19cm^{-3})/Al structure is shown in Fig. 8. In this case, the ZnO:Al/Si stack has been annealed for 15 hours at 600°C for SPC of the silicon. Due to the higher dopand activation in poly-Si compared to a-Si the p-concentration increases about two orders of magnitude. It can be seen, that the curves are not linear any more, indicating a non-ohmic contact. This could be caused by a thin isolating barrier at the interface. Resistances could be calculated by fitting the curve in the quasi linear regime from -0.15 to 0.15V. As the evaluation of a transfer length L_{T*} was afflicted with a big error, again the upper limit for ρ_{CB} was estimated using U_{probe} and I_{TB} to about 320 mΩcm^2 which is in the same order like in the case of ZnO:Al/a-Si(p^+). Again the contribution of ρ_{CT} is negligible.

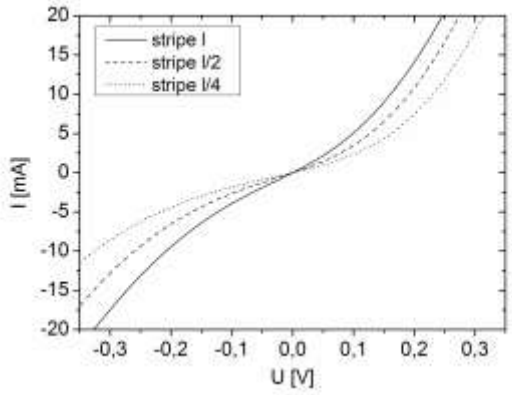

Figure 8: IV-characteristics corresponding to Fig. 7, but after solid phase crystallization of the silicon on ZnO:Al, measured through the ZnO:Al/ poly-Si(p^+)/Al stack with three different Al contact stripe lengths. The resistances have been determined in the quasi linear regime from -0.15 to 0.15V.

Influence of the ZnO:Al surface texture

The contact resistivity of buried ZnO:Al/poly-Si(n^+, ~1E20cm^{-3}) interfaces was investigated for two kinds of surface morphologies of the ZnO:Al film. The first films were in the as-deposited state with a smooth surface, the second films were textured by wet-chemical etching with hydrochloric acid. All contacts were found to be ohmic. By measuring through the whole stack the transfer length L_{T*} for the total contact resistivity $\rho_{CT} + \rho_{CB}$ resulted in 2.08mm and 1.46mm for smooth and textured ZnO:Al, respectively. This yields a total contact resistivity $\rho_{CT} + \rho_{CB}$ of 92 mΩcm^2 for smooth ($R_{sh/ZnO}$ = 2.1Ω) and 45 mΩcm^2 for textured ($R_{sh/ZnO}$ =2.8Ω) layers. As the resistivity of the top contact ranges below 0.1 mΩcm^2 (see Table 1) it can be concluded that the total contact resistivity is dominated by the buried ZnO:Al/poly-Si(n^+, ~1E20cm^{-3}) interface. . The reason for the smaller resistivity of textured layers might be the larger effective interface area.

Influence of a SiN_x diffusion barrier between ZnO:Al and Si

For poly-Si thin film solar cell fabrication a diffusion barrier between ZnO:Al front contact layer and poly-Si material has turned out to be indispensible for a good solar cell performance. As the maximum open circuit voltages for poly-Si thin-film solar cells on ZnO:Al prepared by deposition at 300°C and subsequent SPC at 600°C range below 300mV, the implementation of a 30nm thick SiN_x layer allows for V_{oc} values up to 430mV. A reason for the bad photovoltaic performance without such a barrier could be the diffusion of impurities from the glass substrate and the ZnO:Al layer into the silicon during the high-temperature steps during poly-Si fabrication.
Contact resistivity measurements through ZnO:Al/SiN_x/poly-Si(n^+, ~1E20cm^{-3})/Al layer stacks can be seen in Fig. 9. While the resistance without any barrier is ohmic, the s-shaped IV-characteristics of interfaces with SiN_x-barrier indicate a non-ohmic contact as expected for an isolating barrier at the interface. As an accurate determination of L_{T*} was not possible, ρ_{CB} was overestimated by equation (1) considering a homogeneous flow through the shortest stripes of 1.5mm length. The maximum values for ρ_{CB} increase from about 0.1 Ωcm^2 to 2.6 Ωcm^2 by increasing the SiN_x layer thickness from 0 to 50nm.

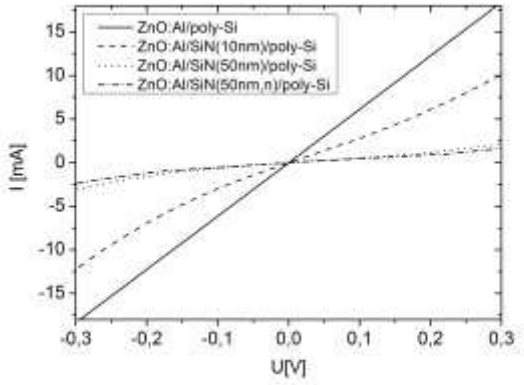

Figure 9: IV-characteristics measured through ZnO:Al/SiN_x/poly-Si(n^+) stacks with 10nm (dashed line), 50nm (dotted line), and 50nm n-doped (dashed-dotted line) SiN barrier layers. The reference without any SiN_x barrier is given by the straight line.

5 Discussion

In order to determine the impact of a contact resistance on the performance of an photovoltaic device, the respective power loss has to be estimated. An upper limit of the relative power loss due to a contact resistivity ρ_C in a solar cell with short circuit current density j_{SC} and open circuit voltage V_{oc} can be estimated by

$$\frac{\Delta P}{P_{\max}} = \frac{\rho_C \cdot j_{sc}^2}{V_{oc} \cdot j_{sc}} = \frac{\rho_C \cdot j_{sc}}{V_{oc}}.$$

Table 2 summarizes the contact resistivity measurements of buried ZnO:Al/SiN_x/poly-Si(n^+, ~1E20cm^{-3}) interfaces for varying SiN_x-thicknesses. While the relative power loss is in a tolerable regime for no or 10nm thick SiN_x layers, the loss due to a 50nm thick SiN_x layer is too high for a decent solar cell performance. For the estimation of the power loss, V_{oc} and j_{sc} values of the best poly-Si thin-film solar cell so far [3] have been taken into account.

barrier	**ρ_C [Ωcm^2]**	**$\Delta P/P_{max}$ [%]**
-	< 0.1	< 0.6
10nm SiN	< 0.37	< 2.2
50nm SiN	< 1.98	< 11.9
50nm SiN(n+)	< 2.57	< 15.4

Table 2: Upper limits for the contact resistivity of a buried ZnO:Al/(SiN_x)/poly-Si(n^+) interface for different SiN_x barrier parameters. The corresponding power loss is estimated for a solar cell with V_{oc}=500mV and j_{sc}=30mA/cm^2.

In summary, the contact resistivities of all measured ZnO:Al/poly-Si interfaces were found to be below 0.4 Ωcm^2 corresponding to a relative power loss below 3%. However, for good solar cell performance an isolating SiN_x diffusion barrier between ZnO:Al and poly-Si is necessary. It was found that the power loss remains in a tolerable regime if the SiN_x is thinner than 10nm.

Conclusion

An experimental technique for the determination of the contact resistivity ρ_C of a buried ZnO:Al/poly-Si interface has been developed by refining an earlier method by Schade and Smith [11].
The influence of a 600°C annealing step, as applied during solid phase crystallization of silicon for thin-film solar cells, on the contact resistivity ρ_C has been investigated. The IV-characteristics show indications for the formation of a thin isolating barrier at the ZnO:Al/Si interface during SPC. However, all measured values of ρ_C range below 0.4 Ωcm^2 corresponding to a relative power loss ΔP below 3% even for the best solar cells.
By texturing the ZnO:Al by wet-chemical etching before Si deposition as done for a better light trapping in the solar cell device, ρ_C can be reduced from about 100 mΩcm^2 to below 50 mΩcm^2 which can be most probably attributed to the bigger effective interface area.
A SiN_x diffusion barrier layer between ZnO:Al front contact and poly-Si has turned out to be necessary for a good solar cell performance. If this SiN_x barrier has a thickness smaller than 10nm the contact resistivity remains below 0.4 Ωcm^2 still resulting in a tolerable power loss.

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